WHAT IS CLAIMED IS:

1. A first-in-first-out memory, comprising:

a memory array;

a clock terminal for receiving a clock signal;

a write enable terminal for receiving a write enable signal;

inputs for receiving input data words;

a read enable terminal for receiving a read enable signal;

outputs for presenting output data words of the same word width as that of the input data words;

a write buffer, coupled to the inputs and to the array of memory cells, for receiving a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, and for writing the first and second input data words to the memory array in a single write cycle;

read circuitry, for requesting a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and

a read buffer, for receiving first and second output data words from the memory array responsive to the request of the read of the memory array, and for presenting the first and second output data words in sequence to the outputs.

2. The memory circuit of claim 1, wherein the write buffer comprises:

a plurality of buffer storage locations; and

sequential logic, for controlling the write buffer to store input data words received from the inputs in selected ones of the buffer storage locations, and for controlling the write buffer to forward pairs of stored input data words to the memory array.

3. The memory circuit of claim 2, wherein the plurality of buffer storage locations are arranged in rows and columns, including first and second columns of buffer storage locations having storage locations in first and second rows.

4. The memory circuit of claim 3, wherein the sequential logic controls the write buffer to store a first input data word in a buffer storage location at the first row and the first column, and to store a second input data word in a buffer storage location at the second row and the first column;

and wherein the sequential logic also controls the write buffer to then forward the first and second input data words to the memory array in an internal write cycle.

5. The memory circuit of claim 4, further comprising:

a clock input for receiving a periodic clock signal; and

clock circuitry, for assigning alternating cycles of the periodic clock signal as internal write and internal read cycles.

6. The memory circuit of claim 5, wherein the sequential logic also controls the write buffer to then store a third input data word in a buffer storage location of the second column responsive to the inputs receiving the third input data word prior to an internal write cycle.

7. The memory circuit of claim 1, wherein the read buffer comprises:

an output width converter, for converting double-width output data words read from the memory array into a sequence of output data words; and

an output FIFO, coupled to the output width converter, for buffering the output data words in a first-in-first-out fashion.

8. The memory circuit of claim 7, wherein the read circuitry further comprises:

an output register for presenting an output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal.

9. The memory circuit of claim 7, wherein the output FIFO generates a read ready signal responsive to its contents storing a number of output data words exceeding a first threshold.

10. The memory circuit of claim 9, wherein the output FIFO generates a stop read signal to the memory array responsive to its contents storing a number of output data words exceeding a second threshold that is higher than the first threshold;

and wherein the output FIFO generates a start read signal to the memory array responsive to its contents storing a number of output data words below a third threshold that is lower than the first threshold.

11. The memory circuit of claim 1, wherein the input data words and output data words correspond to data arranged in packets, each packet including a start-of-packet indicator and an end-of-packet indicator;

and further comprising:

packet management logic, for controlling the operation of the memory circuit, the packet management logic for enabling the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator.

12. The memory circuit of claim 12, wherein the packet management logic is also for enabling the outputting of output data words corresponding to a jumbo packet, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

13. The memory circuit of claim 11, wherein the packet management logic is also for maintaining a count of the number of packets stored in the memory array.

14. The memory circuit of claim 13, wherein the packet management logic is also for disabling the outputting of output data words, responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.

15. The memory circuit of claim 14, wherein the read buffer comprises:

an output width converter, for converting double-width output data words read from the memory array into a sequence of output data words;

an output FIFO, coupled to the output width converter, for buffering the output data words in a first-in-first-out fashion; and

an output register for presenting an output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal.

and wherein the packet management logic controls the output register to disable the outputting of output data words responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.

16. A method of buffering data words with a memory circuit, comprising the steps of:

receiving a sequence of input data words at input terminals of the memory circuit;

responsive to receiving a first input data word and a second input data word, writing the first and second input data words into a memory array of the memory circuit in a single write cycle;

receiving read strobe signals;

responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle;

sequentially presenting the first and second output data words at output terminals of the memory circuit.

17. The method of claim 16, further comprising:

responsive to receiving an input data word, storing the input data word in a write buffer having a plurality of buffer storage locations arranged in rows and columns, each column having first and second buffer storage locations associated with first and second rows, respectively;

and wherein the writing step is performed responsive to the first and second buffer storage locations of a first column storing the first and second input data words, respectively.

18. The method of claim 17, further comprising:

receiving a periodic system clock signal; and

assigning internal write cycles and internal read cycles to alternating ones of an internal clock corresponding to the system clock signal.

19. The method of claim 18, wherein the writing step is performed responsive to the first and second buffer storage locations of the first column storing the first and second input data words, respectively, in combination with an internal write cycle.

20. The method of claim 19, further comprising:

receiving a third input data word; and

responsive to receiving the third input data word and to the first and second buffer storage locations of the first column storing the first and second input data words, respectively, and prior to an internal write cycle, storing the third input data word in a buffer storage location of a second column.

21. The method of claim 16, further comprising:

after the reading step and prior to the presenting step, buffering the first and second output data words in an output FIFO buffer; and

before the presenting step, generating a read ready signal responsive to the output FIFO buffer storing a number of output data words exceeding a first threshold;

and wherein the presenting step is performed responsive to receiving a read strobe signal after the generating of the read ready signal.

22. The method of claim 21, further comprising:

generating a stop read signal to the memory array responsive to the output FIFO buffer storing a number of output data words exceeding a second threshold that is higher than the first threshold; and

generating a start read signal to the memory array responsive to the output FIFO buffer storing a number of output data words below a third threshold that is lower than the first threshold.

23. A method of managing the communications of data words arranged in packets, each packet of data words including a start-of-packet indicator and an end-of-packet indicator;

receiving a sequence of input data words at input terminals of the memory circuit;

responsive to receiving a first input data word and a second input data word, writing the first and second input data words into a memory array of the memory circuit in a single write cycle;

responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet;

receiving read strobe signals;

responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle; and

sequentially presenting the first and second output data words at output terminals of the memory circuit.

24. The method of claim 23, further comprising:

enabling the output of data words corresponding to the packet, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

25. The method of claim 23, further comprising:

incrementing a count of the number of packets stored in the memory array responsive to detecting the writing of an end-of-packet indicator.

26. The method of claim 25, further comprising:

disabling the outputting of output data words, responsive to the outputting of an end-of-packet indication for a packet and to the count indicating that no additional packets are stored.

27. The method of claim 26, wherein the disabling step comprises:

controlling an output register to disable the presenting of output data words at the output terminals.

28. A network node for controlling the transmission and receipt of packet-based data over a communications facility, comprising:

a system interface for receiving transmit data from a system and for outputting processed received signals to the system;

a transmit FIFO buffer, for buffering transmit data received at the system interface;

a transceiver, for driving the communications facility with transmitted signals corresponding to the transmit data, and for receiving signals from the communications facility;

a receive FIFO buffer, for buffering the received signals; and

wherein each of the transmit and receive FIFO buffers comprise:

a memory array;

a clock terminal for receiving a clock signal;

a write enable terminal for receiving a write enable signal;

inputs for receiving input data words;

a read enable terminal for receiving a read enable signal;

outputs for presenting output data words of the same word width as that of the input data words;

a write buffer, coupled to the inputs and to the array of memory cells, for receiving a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, and for writing the first and second input data words to the memory array in a single write cycle;

read circuitry, for requesting a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and

a read buffer, for receiving first and second output data words from the memory array responsive to the request of the read of the memory array, and for presenting the first and second output data words in sequence to the outputs.

29. The network node of claim 28, wherein the transceiver comprises:

a serializer, for serializing the transmit data;

a line driver, for driving the communications facility with serial signals from the serializer;

a receiver, for receiving serial signals from the communications facility; and

a deserializer, for deserializing the signals received by the receiver.

30. The network node of claim 28, further comprising:

a transmit media access control function, for processing the transmit data buffered by the transmit FIFO buffer; and

a receive media access control function, for processing the received signals and applying the processed received signals to the receive FIFO buffer.

31. The network node of claim 28, wherein the write buffer in each of the transmit and receive FIFO buffers comprises:

a plurality of buffer storage locations arranged in rows and columns, including first and second columns of buffer storage locations having storage locations in first and second rows; and

sequential logic, for controlling the write buffer to store a first input data word in a buffer storage location at the first row and the first column, and to store a second input data word in a buffer storage location at the second row and the first column, and to then forward the first and second input data words to the memory array in an internal write cycle.

32. The network node of claim 31, wherein the write buffer in each of the transmit and receive FIFO buffers comprises:

a clock input for receiving a periodic clock signal; and

clock circuitry, for assigning alternating cycles of the periodic clock signal as internal write and internal read cycles;

wherein the sequential logic also controls the write buffer to then store a third input data word in a buffer storage location of the second column responsive to the inputs receiving the third input data word prior to an internal write cycle.

33. The network node of claim 28, wherein the read buffer in each of the transmit and receive FIFO buffers comprises:

an output width converter, for converting double-width output data words read from the memory array into a sequence of output data words; and

an output FIFO, coupled to the output width converter, for buffering the output data words in a first-in-first-out fashion.

34. The network node of claim 33, wherein the read circuitry further comprises:

an output register for presenting an output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal.

35. The network node of claim 33, wherein the output FIFO generates a read ready signal responsive to its contents storing a number of output data words exceeding a first threshold.

36. The network node of claim 35, wherein the output FIFO generates a stop read signal to the memory array responsive to its contents storing a number of output data words exceeding a second threshold that is higher than the first threshold;

and wherein the output FIFO generates a start read signal to the memory array responsive to its contents storing a number of output data words below a third threshold that is lower than the first threshold.

37. The network node of claim 28, wherein each packet of data words includes a start-of-packet indicator and an end-of-packet indicator;

and wherein each of the transmit and receive FIFO buffers further comprise:

packet management logic, for controlling the operation of the memory circuit, the packet management logic for enabling the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator.

38. The network node of claim 37, wherein the packet management logic is also for enabling the outputting of output data words corresponding to a jumbo packet,

responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

39. The network node of claim 37, wherein the packet management logic is also for maintaining a count of the number of packets stored in the memory array.

40. The network node of claim 39, wherein the packet management logic is also for disabling the outputting of output data words, responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.

41. The network node of claim 40, wherein the read buffer comprises:

an output width converter, for converting double-width output data words read from the memory array into a sequence of output data words;

an output FIFO, coupled to the output width converter, for buffering the output data words in a first-in-first-out fashion; and

an output register for presenting an output data word received from the output FIFO at the outputs, in combination with a data valid signal, responsive to the read circuitry receiving a read enable signal.

and wherein the packet management logic controls the output register to disable the outputting of output data words responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored.

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